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The standard FPGA design flow starts with design entry using schematics or a hardware description language (HDL), such as Verilog HDL or VHDL In this step, you create the digital circuit that is implemented inside the FPGA The flow then proceeds through compilation, simulation, programming, and verification in the FPGA hardware (see Figure 1

HDL Synthesis for FPGAs Design Guide

FPGA system features and is structured into hierarchical blocks These topics are described in detail in this manual HDL Synthesis Floorplanning Work Flow RTL HDL Simulation Functional Gate-level Simulation Timing Gate-level Simulation X4915 Structured ...

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